REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

This Standard is divided into sections; these sections define DEK's PCB requirements in the areas of design, build, test, materials and data. Each section is stand-alone and hence the document can be invoked in sections or as a whole.

SECTION 1 - DESIGN REQUIREMENTS

1.1 Overview

This standard engineering instruction defines the design requirement that must be applied for all circuit boards designed at or commissioned by DEK Printing.

1.2 General Rules

All design to be performed in line with requirements of IPC standards within the 2200 series, key standards being:-

- IPC 2221 Generic Standard on Printed Circuit Board Design

Specific design standards exist for certain board structures, type these are defined within IPC 2221, typically:-

- IPC 2222 Sectional Design Standard for Rigid Organic Printed Boards.
- IPC-SM-782 Surface Mount design and Land Pattern Standard

Where Assembly or board layout drawings are produced then they should conform to the requirements of:-

- IPC-2615 Printed Circuit Board Dimensions and Tolerance.

Contractual documents can override the requirements of this standard, but any such exceptions must be documented and justified within the contract documents.

1.3 Design Requirements, Clarifications and Exceptions

Clarification or variation to ***numbered*** sections of standard IPC 2221

Section 1.6.3 Productibility level

There is no outline requirement for the production and supply of GA drawings for product. GA drawings are a requirement only where complex or unusual assembly or board characteristics are required. Boards need to be manufactured to workmanship standard defined in BUILD AND ASSEMBLY REQUIREMENTS section of this DSEI

Section 3.2 Design layout

Design review should be conducted at least once pre and once post design, layout. Personnel from the following areas should be included.

- DEK

- Design
- Production Engineering.
- Purchasing.
- Design Consultants
- Board Assembly Manufacturer

Section 3.5.6.1 Bare Board Testing

Bare Board Testing and inspection to be performed on 100% of volume production product (volume = more than 25 pieces). Physical parameters are also to be checked.
Preferred test method - Intelligent test carried out against board net listing
Non preferred method - Comparative test against golden board.

Section 4.1 Board Material

Board material to match bare board's requirement as defined in Bare Board section of this DSEI.

Section 4.6 Legend and marking

To be screened onto all boards, Items requiring identing :-

- DEK PCB assembly number
- Bare Board Issue status (In Copper)
- Description,(typically - 'ES Interface')
- Component ID'S
- Component foot prints
- Component polarising and key pin idents
- Board base material approvals, UL, etc

Section 5.2.4 Bow and Twist

Defined in Build and Assembly section of this DSEI

Section 6.3 Electrical Clearance

All designs to match or exceed the requirements of UL standards, clearance distances shall be specified as the larger clearance selected from the relevant IPC design standard or the requirements of BS EN 60950 Section 2.9. Whichever offers the highest distances.

Section 10.1.2 Electrical Creepage

All designs to match or exceed the requirements of UL standards, creepage distances shall be specified as the larger distance selected from the relevant IPC design standard or the requirements of BS EN 60950 Section 2.9. Whichever offers the highest distances.

1.4 Documents for DEK to Issue Pre Layout.

- Contract
- Purchase Order
- Relevant DSEI documents

- Board requirement documents
- Physical constraints, size, component area, etc.
- Critical Components Lists (data on key components, including manufacturer part no.)
- Circuits
- Node list/tracks list detailing
- Voltage current and signal requirements per line
- Special assembly requirements
- Change process definition
- Product marking
- Test Requirements

1.5 General Notes

Units of measure

- Sl units
- mm for length measure
- Celsius temperature

Marking and Identification of Development Product, all boards to be marked with the following as a minimum :-

- DEK assembly number
- Issue status
- Serial number
- Description
- Label clearly defining development product, source and manufacture date

1.6 Documents Required by DEK Post Design.

All documents should be electronic file format, issued on CD ROM or emailed as a design package on a “per product” basis:-

- Design Source File
- Gerber Files
- SMA ASCII text files containing circuit ref. X, Y, & Theta co-ordinates + side panel
- Drilling Data
- Routing Data
- Special Test Requirements
- Special Tooling Requirements
- Full Parts List
- Special Assembly notes
- Node list / tracks list detailing, voltage current and signal requirement
- Step and repeat data

REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

SECTION 2 - BARE BOARD MATERIAL SPECIFICATION

2.1 Overview

This standard engineering instruction defines the requirement for base materials, (material bare board are manufactured from) and bare board construction criteria.

2.2 Aim

The aim of this document is to define reference standards and specific construction requirements to be applied in build of DEK bare boards.

2.3 Base Materials

2.4 General

Base material to be as the requirement defined in IPC standards:-
IPC-4101 Material for Base Materials for Rigid and Multi-layer Printed Circuit Boards.

Acceptability of the bare board to be in accordance to IPC-A-600

Where conflicts occur, the requirement of this document or any other DEK standard or procedure take precedence over the above IPC document.

The particular materials required will be dependent upon board style, performance and application. Details of the material selected (in consultation with supplier) to be defined within particular boards inception document / design file.

Contractual documents can override the requirements of this standard, but any such exceptions must be documented and justified within the contract documents.

2.5 Clarification of and Exceptions to IPC-4101

2.5.1 Flammability

Laminates and finished boards must meet the requirements of UL94 and must have ratings of UL94V-0 for flammability.

The DEK requirement is for V-0 Class materials as specified in section 1.2.13 of BS EN 60950 Safety of Information Technology Equipment Including Electrical Business Equipment.

2.5.2 Surface Finish

Determined by:-

a. Existing design / product prior to 01/07/2006
b. New design / product after 01/07/2006 RoHS compliant

2.5.2.1. Existing design product prior to 01/07/2006

Standard surface finish requirements
- Alpha Level silver
- Special finished to be defined as required

Note. Finishes will be specified in the board 'Requirement Specification'

2.5.2.2. New design / product after 01/07/2006 (RoHS compliant)

Standard surface finish requirements
- Electroless Nickel (Ni) thickness of 3-6 microns, with a flash of Gold (Au) 0.05 microns (min), as stated in IPC 4552 for Class 1, 2, and 3. ENIG
(ENIG = Electroless Ni, Immersion Gold)

As an alternative if the ENIG process is not available it is permissible to use :-
- Electroless Nickel (Ni) thickness of 3-6 microns, with a flash of Silver (Ag) 0.05 microns (min), as stated in IPC 4553 Thin Silver for Class 1, 2, and 3. Or with a flash of Silver (Ag) 0.12 microns (min), as stated in IPC 4553 Thick Silver for Class 1, 2, and 3.

Note. Finishes will be specified in the board 'Requirement Specification'.

2.5.3 Legends and Marking

To be printed using white inks on both sides of the board as required indicating:-
- DEK assembly number
- Bare Board Issue status
- Description (typically - 'ES Interface')
- Component ID'S
- Component foot prints
- Component polarising and key pin idents
- Board base material approvals, UL, etc.

2.5.4 Bare Board Testing

Bare Board Testing to be an intelligent test carried out against net listing on 100% of product. Physical parameters to also be checked

2.5.5 Physical Constraints

Bow and Twist, should be to a maximum of 1% of boards longest edge, typically 1mm on a 100mm board

Meaning on a 1.6mm thick board, laid flat on a surface table the maximum deviation above the surface of the table would be 2.6mm

Test methods as defined in IPC-TM-650

REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

SECTION 3 - DATA FOR MANUFACTURE

3.1 Overview

This standard engineering instruction defines the data to be issued to current and prospective board assembly manufacturers.

3.2 Aim

The aim of this document is to ensure that all necessary and relevant data is supplied to the PCB manufacturer. And that all DEK requirements are clearly defined.

3.3 General Rules

Data to be issued in line with requirement defined in IPC standards:-

IPC-D-326 Information Requirements for Manufacturing printed Circuit Board Assemblies.

Where conflicts occur the requirement of this document or any other DEK standard or procedure, DEK documents take precedence over the above IPC document.
The suite of data issued will be dependent upon board style, performance and application. A standard documents listing sheet to be completed as per sheet 2 of this document.
Contractual documents can override the requirements of this standard, but any such exceptions must be documented and justified within the contract documents.

3.4 Clarification of and Exceptions to IPC-D-326

Clarification or variation to ***numbered*** sections of standard IPC-D-326

Section 4.1

All materials to be supplied by assembler, unless otherwise specified in contractual documentation.

Section 4.8

A full quality and manufacturing audit should be performed on any supplier pre order placement, any specific quality issue for correction to be documented, issues to be resolved pre order placement or product supply.

Section 4.10

Requirement is to define any standard engineering requirements as well as any specific product related items.

Section 6.1

Assembly drawings are only required for complex or non-standard assembly requirements, when available they should be provided as part of the documentation package.

REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

Section 6.3
See comments on section 6.1 above

3.5 Document List

Listing of documents to be issued with every board enquiry placed.
Template is available, showing typical listing as below.

PCB Assembly Number : -			
Document ID	Description	Date of issue	Issue status
	BOM (including parts specifications)		
	Assembly identifications requirements		
	Document listing		
	Test requirements		
	Programmable device data (If applicable)		
	Packaging requirements		
	Manufacturing Gerber Files		
	Quality System Evaluation (Including upgrades required)		
	ESS requirements (ESS – Environmental Stress Screening)		
	Workmanship Standards (DSEI document and board specific listing)		
	Models and assembly drawings		
	Delivery requirements		
	Contractual documents (Including copy exact)		
	ASCII text file (For SMA's)		

REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

SECTION 4 - BUILD AND ASSEMBLY REQUIREMENTS

4.1 Overview

This standard engineering instruction defines the documentation requirements and assembly standards that must be achieved in production of all DEK circuit board assemblies.

4.2 General Rules

All manufacturing to be performed in line with requirements of IPC standards -

- IPC / ELA J-STD-001E Requirements for Soldered Electrical and Electronic Assemblies
- IPC-A-610 Acceptability of Electronic Assemblies

Documentation to be supplied in line with the requirements outlined in Data for Manufacture section of this DSEI.

4.3 General Requirements

DEK will supply documentation generally in line with IPC - D - 326, with the clarification of:-

4.3.1 BOM's

- The vendor will supply all materials required.
- All materials / components used will be from the manufacturers specified.

4.3.2 Control Documents

DEK will issue the following documents as required, to detail build and requirement.

- Parts Lists
- Gerber Files
- SMA ASCII text files containing circuit ref. X, Y, & Theta co-ordinates + side panel.
- Circuits
- GA's (for special or complex assemblies or assembly operations)
- PIC code.

4.3.3 Testing and Test Equipment

- Test requirement and test equipment to be defined in board test document.
- Test equipment to be supplied by vendor. Method of supply and allocated costs to be defined at the initiation of any new board contract.

4.3.4 Quality System

- Supplier shall operate an approved quality system in line with ISO 9001 2000

4.3.5 Workmanship Standards

Suppliers are required to supply to the following standards these are listed in order of precedence –

- Special instruction in GA's or other DEK specific data.

- IPC / ELA J-STD-001E Requirements for Soldered Electrical and Electronic Assemblies
- IPC - A - 610 Acceptability of Electronic Assemblies.

Workmanship of assemblies to be to Class 2 levels as defined in IPC / ELA J-STD-001E section 1

Exceptions and variation to the build class to be assessed and defined on a per board basis at the time of introduction, with in the 'Board requirement document'.

4.3.6 Quantity and Delivery Requirements

To be defined by purchasing, items to cover include -

- Contractual and purchase order requirements.
- Delivery requirements, line side and JIT as applicable.

4.3.7 Design Change Process

No change to be made in the areas listed below without approval of DEK and change approval via the DEK DCR process.

- Components
- PCB layout, component arrangement and clearance and Creepage distances.

4.3.8 Marking and Identification

All boards to be marked with the following as a minimum :-

- DEK assembly number
- Issue status
- Serial number
- Board description

4.3.9 Build Clarifications and exceptions

PCB build will be to the standards defined in :- IPC /ELA J-STD-001E (Requirements for soldered electrical and electronic assemblies).
Inspection and workmanship quality shall be reviewed in line with :- IPC-A-610 (Acceptability of electronic assemblies).

4.3.10 Units of measure

SI Units

- Mm for length measure
- Celsius for temperature

4.3.11 Process control measurement

Process should be monitored and evaluated with various measures :-

- Monitoring of process indicators
- In process reject analysis
  - 1st time pass rates

- 2nd time pass rates

- Customer returns reject analysis
- Process changes to be documented and validated
- Statistical process control systems are to be evident and functional within the standard process control envelope
- SPC Analysis should be performed in line with the methodology presented in the IPC manufacturing standard

4.3.12 Solder

Shall be in accordance with J-STD-006 (Requirements for Electronic Grade Solder).

4.3.13 Flux

Shall be in accordance with J-STD-004 ((Requirements for Soldering Fluxes).
"No Clean" Fluxes may be used; when used the detail should be listed within the "Board requirement document".

4.3.14 Cleaning

All boards to be cleaned unless assembled using "No Clean" Fluxes, method and testing requirements to be defined on a "per product" basis and discussion with supplier. Items for discussion include:-

- Sides of board to be cleaned
- Solder type used
- Testing of effectiveness of cleaning process. (Batch test)
- Possibility of no cleaning if "No Clean" fluxes used
- Component compatibility for "Bath" and or "Immersion" cleaning
- Type of cleaning fluid to be used / specified

4.3.15 Inspection

100% inspection required on all new boards.

- This to be performed to a defined requirement.
- Relaxation of inspection requirement only to be undertaken after documented review of defect analysis data and proving of suitability of change.

4.3.16 Physical Constraints

Bow and Twist, should be to a maximum of 1% of boards longest edge,

- Typically 1mm on a 100mm board.
- Meaning on a 1.6mm thick board, laid flat on a surface table the maximum deviation above the surface of the table would be 2.6mm
- Test methods as defined in IPC-TM-650

4.3.17 Coatings and Encapsulates

- All boards to be supplied un-coated, unless such is required with the specific product build data.

• When specified coating and encapsulate shall be used in line with both the defined IPC standard and the material manufacturer, or DEK's product specification documentation.
• Hierarchy of documents is:-
    • DEK specific work / instruction procedures
    • Material manufacturer's instructions, (usage, not coverage)
    • IPC procedures.

4.3.18 Repairs and "Up Issue modifications"

• No repair / up issue / modification of any DEK product is permissible without written approval.
• When work is approved then it is to be carried out in line with the requirements specified in IPC-7721 Repair and Modification of Printed Circuit Board and Electronic Assemblies.

4.3.19 Rework

• Rework of DEK product is permissible but defect must be documented and process corrections made to ensure problems do not re-occur.
• Any rework undertaken, to be reviewed within the product returns process and review with DEK.
• Rework to be carried out in line with the requirements specified in IPC-7721 Repair and Modification of Printed Circuit Board and Electronic Assemblies.

4.3.20 General Requirements

Items of clarification or requirement not defined elsewhere.
• All component placement, soldering, wire laying etc. should be done such that no reduction in the designed in clearance / creepage distance is introduced at the assembly / build process.

REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

SECTION 5 - TEST REQUIREMENTS

5.1 Overview

This standard engineering instruction defines standard test and inspection requirement that can be applied to PCB assemblies. Due to the large diversity of assembly types used, varying from simple point-to-point connection boards, to active power switching control boards, hence there are various test profiles defined below. The specific test requirement for each board is to be defined and expanded with in the 'REQUIREMENT SPECIFICATION' for the individual product.

5.2 General

All testing and all fixtures, fittings and instructions associated, must be controlled updated and maintained within a functional traceable environment, all run under the control of the prevailing ISO quality system.

All processes should be monitored and evaluated using SPC tools.

5.3 Test Equipment

Programming of automated test equipment and design and control of all equipment must be through quality control systems.

All testing will be done with either:-
- Automated test equipment.
- Custom functionally operational test equipment.

Test equipment will also have the following attributes:-
- Test equipment must be controlled and calibrated.
- Test software must be tamper protected.

5.4 Test logs

- All tests should be logged.
- Each board tested should be traceable to a test date, serial number and operative.
- An internal review of failure modes and corrective action should be undertaken periodically. Any issues requiring potential design change should be fed back to DEK

5.5 Test 'PCB T1'-Visual Inspection

Bare Boards tested and inspected to 'Bare Board Section' of this document.
Assembled Board Inspection
- 100% inspection required on all new boards.
- This to be performed to a defined requirement.

Relaxation of inspection requirement only to be undertaken after documented review of defect analysis data and proving of suitability of change.

This test requires the test / inspection operative to perform a visual inspection of the PCB presented for test. Typical items to be tested checked are:-

- General check for abrasions or any signs of damage or contamination.
- All relevant legends, number and labelling are fitted and legible.
- Board matches the criteria of standard IPC-A-610 C in respect to build requirements.
- All screws, covers, heat sinks, fitted correctly and secure.
- Any adjustable on board items, can be adjusted.
- Check manufacturer's part reference to ensure correct parts supplied and used.
- Any specific inspection criteria defined within the board test requirement document are correct.

5.6 Test 'PCB T2'-In Circuit Testing

A method of probing a board and determining that the correctly profiled components are fitted.

- Method and requirement to be defined with supplier.

5.7 Test 'PCB T3' - ATE Node Testing

Automated test of node point connection and isolation, can also in some cases be used to detect simple component on board when configured to provide non-complex / active circuits, typically detect diode, resistors capacitors both in and across the node point connection. Test parameters need to be defined with supplier.

Typical test parameters to be applied:-

- Short circuit node-to-node track test resistance less than 1ohm within board assembly.
- Open circuit resistance between nodes and track to be greater than 1 M ohm within board assembly.
- For diodes, resistors, capacitors, inductors etc, value will be dependent on component and set to detect the required value ± the manufacturer + 1%.
- ATE node testing to be performed by plugging directly into the board's external mounting connectors.

5.8 Test 'PCB T4' - Functional Testing

This may be performed either by the use of interactive ATE equipment that has the capability to drive the product in the manner in which it would be used within the machine environment, or by the construction of suitable custom test jigs and fixtures. The key requirement is that the testing performs a representative test of the true and final operating environment.

- Supply voltage matches those in final use.
- Monitor signal input and output speed and level are consistent with the final operating environment.
- Results are parameter based and not straight pass or fail.
- Status changes for outputs and inputs are applied and monitored.
- Operation is checked at extremes of window of operation.
- Operation of on board test points is correct.
- Correct operation of any on-board indicators or LED's

5.9 Test 'PCB T5' - Environmental Stress Screening

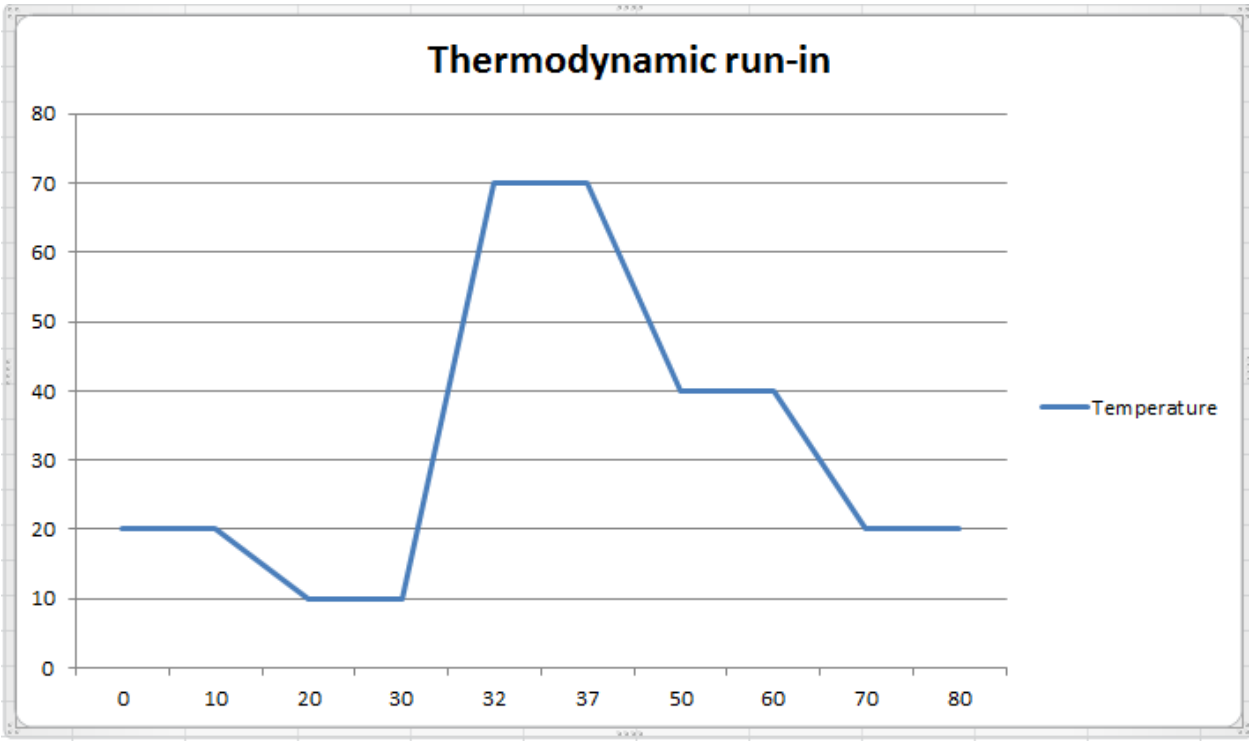
Below is defined an ESS or Thermodynamic run-in process for burn in of PCB's.

REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

General notes:-

- These tests to be performed at Vendors premises as part of full test and inspections program.
- Functional, ICT or ATE testing to be specified as the active element of the test.
- Components on assemblies under test must not exceed their maximum permitted temperature. (In special cases if required test parameter to be redefined on per unit basis to accommodate)



Clarification of Graph

- 20C used as a demonstration of typical Room temperature, use prevailing room temperature in place of 20C specified.
- All areas of board and components must be stable and soaked at 10C before the rise to 70C is initiated.
- Time elements are non-critical with the exception of the 10 to 70 degree rise time period, which must be achieved with a rise rate of circa 30C per minute.
- All areas of board and components must be stable and soaked at 70C before the fall to 40C is initiated.
- Selected method of test to be initiated when the unit is stable at 40C, and continue as the temperature falls to room ambient.

5.10 Post Test Requirements

REQUIREMENTS FOR PCB'S FOR PRODUCTION

DSEI-PCB

- Failing units to be positively marked and segregated for evaluation of the failure mode, marking to include failure mode and temperature at which failure occurred.
- Failing units can be reworked in accordance with the DEK Supplier Quality Assurance Requirements for PCBAs (Q039). This refers to the relevant IPC standards.
- Passing unit to be marked T5