ASMPT enabling the digital world

SIPLACE CA2

High-speed chip assembly directly from wafer and SMT placement in one machine

SMT AND DIE BONDING:
SIPLACE CA2

THE HYBRID SIPLACE CA2 HIGH-SPEED PLATFORM REVOLUTIONIZES SiP PRODUCTION

Only consistent miniaturization and increasingly complex electronics make things like smart devices, autonomous driving and the 5G communication standard possible. The key technology is System in Package (SiP) because it combines ICs and SMT components into a compact, highly innovative system.

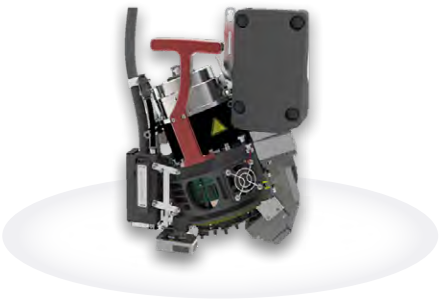
As a hybrid combination of a SMT placement machine and a die bonder, the new SIPLACE CA2 can process SMDs supplied from changeover tables and feeders as well as dies taken directly from a sawn wafer in a single workstep. By integrating the complex die bonding process into the SMT line it eliminates the need for special machines in production. Reduced personnel deployment, high connectivity and integrative data utilization make the new SIPLACE CA2 the perfect match for the Intelligent Factory.

Placement directly from the wafer: more cost-effective and sustainable

Direct placement from the wafer eliminates the entire die taping process. The result: less replenishment or splicing, less effort to feed material to the line. Eliminating the tape feed for the sensitive dies also reduces handling risk and increases production resiliency. All of these factors add up to a significant reduction in costs. At the same time, taping waste is eliminated, making the manufacturing more environmentally friendly and sustainable overall, while increasing ROI.

Flexible combination

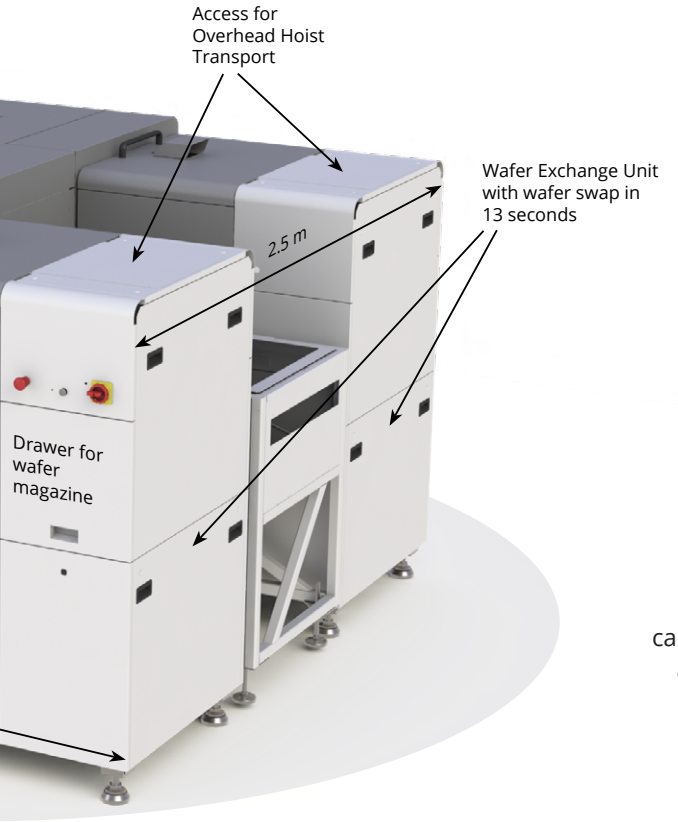
SMT and die bonding in one line simplify your process flow and improve material logistics.



Placement Head CP20

- Component spectrum: 0201metric to 8.2 mm × 8.2 mm × 4 mm
- Touchless pickup and placement
- Placement force: 0.5 N – 4.5 N
- Extremely fast: Up to 38,000 cph
- Extremely precise: Up to ±10 µm @ 3 σ

MULTITALENT COMBINES
TWO WORLDS IN ONE MACHINE



Maximum productivity

Processes SMT components and dies directly from the wafer with die-attach and flip-chip processes in the same work step.

Cost-saving

No taping cost, no associated quality cost of the die taping process and no efforts for tape-waste disposal. Left In Left Out conveyor feature allows for single-sided substrate handling.

Unique flexibility

Wafer system for up to 50 different wafers with a wafer swap time of less than 10 seconds (“full multi-die capability”). A wafer chuck, flux (linear) dipping unit (LDU) and 10 × 8 mm tape-and-reel feeder tracks can be used parallel to pick up from wafer.

Full traceability

Keep track of data for each die from its source on the wafer to its placement position on the circuit board (“full single-die-level traceability”).

Consistent sustainability

Processing dies directly from the diced wafer eliminates the entire die-taping process – and lots of tape waste.

Maximum performance

Thanks to die buffering and process parallelization, the SIPLACE CA2 can place up to 54,000 components per hour directly from wafer with an accuracy of up to 10 µm @ 3 σ.

Comprehensive quality management

Multiple high-end vision system reliably recognize even the smallest components and elements for comprehensive process control.

Wafer Exchange Unit

- Extremely flexible: Processes up to 50 different wafers
- Extremely fast: Wafer swap in only 13 seconds

More about
SIPLACE CA2

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Placement speed (benchmark)	SMT up to 76,000 cph Flip chip from wafer up to 51,000 cph Die attach from wafer up to 54,000 cph
Wafer swap	13 seconds
Placement accuracy (3 σ)	20 µm / 15 µm / 10 µm (can be selected on placement position and component shape level)
PCB dimensions (l × w) dual lane conveyor	50 mm × 45 mm to 375 mm × 260 mm (20 µm) 50 mm × 45 mm to 375 mm × 430 mm (20 µm) (dual as single lane mode) 50 mm × 55 mm to 250 mm × 100 mm (15 µm) 50 mm × 55 mm to 250 mm × 100 mm (10 µm)
PCB dimensions (l × w) single lane conveyor	75 mm × 55 mm to 700 mm × 620 mm (20 µm) 75 mm × 55 mm to 700 mm × 620 mm (15 µm) 75 mm × 55 mm to 700 mm × 620 mm (12 µm) (per 300 mm × 300 mm quadrant) 75 mm × 55 mm to 300 mm × 300 mm (10 µm)
Machine dimensions (l × w × h)	2.56 m × 2.50 m × 1.85 m
Feeder slots	up to 80 × 8-millimeter tape-and-reel feeder or up to 2 × Multi Wafer System and 10 × 8-millimeter tape-and-reel feeder
Power consumption (average)	1.9 kW
Air consumption	120 Nl/min (2 × SIPLACE CP20)
Certifications	CE, SEMI S2/S8, Clean room class ISO 7
Data interfaces	IPC-HERMES-9852, IPC-CFX, IPC-SMEMA-9851, SECS/GEM

Placement head	SIPLACE CP20
Component range	from tape-and-reel: 0201m up to 8.2 mm × 8.2 mm from wafer: 0.3 mm × 0.3 mm up to 8.2 mm × 8.2 mm
Min. lead pitch	70/50* µm
Min. lead width	30/25* µm
Min. ball pitch	100/50* µm
Min. ball diameter	50/25* µm

* with optional high-resolution camera (SST49)

ASMPT

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