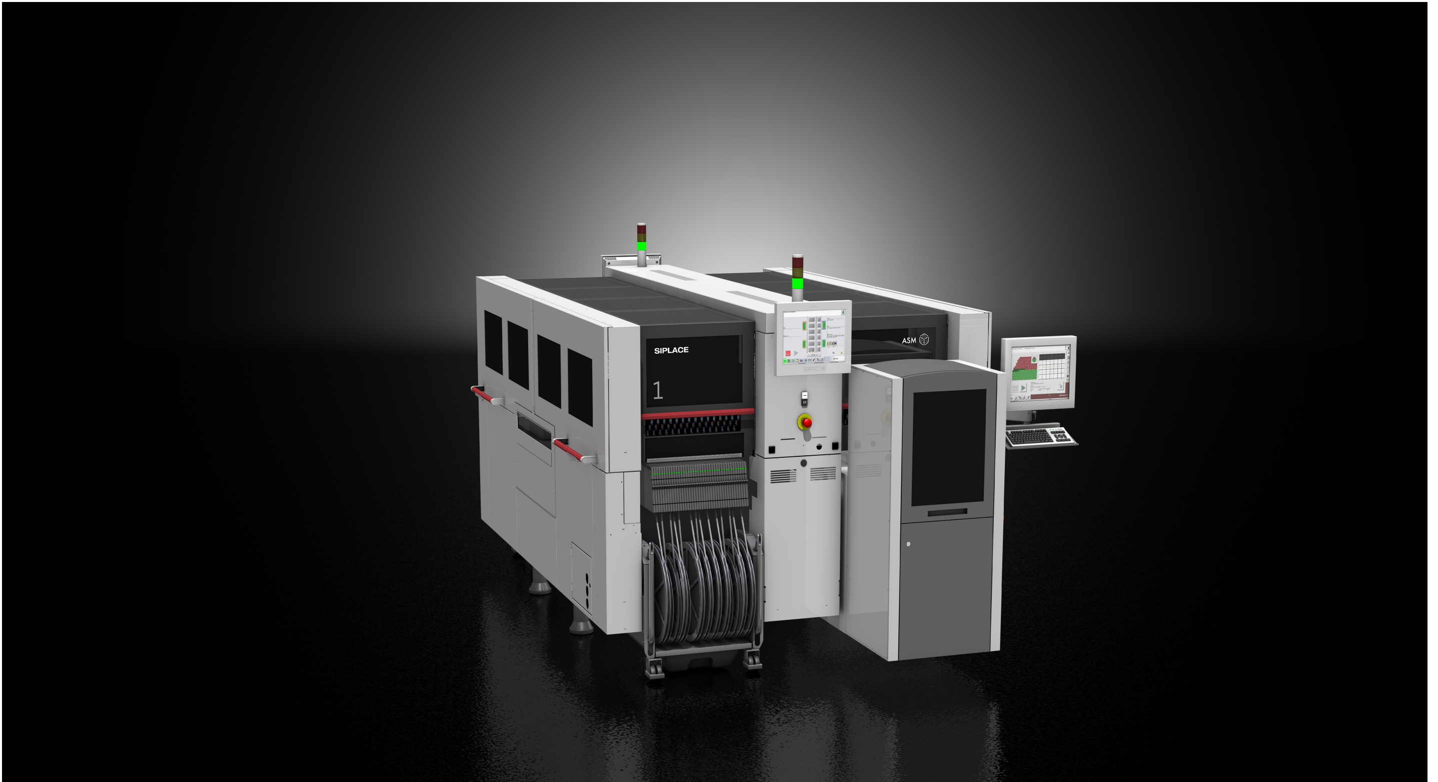
SIPLACE CA

Highest Accuracy for Advanced Packaging



The SIPLACE CA (Chip Assembly) platform can place bare dies directly from wafers using the die attach or flip chip process. It supports the full range of SMT placement capabilities provided by the SIPLACE X Series. The SIPLACE CA can be used for direct die attach or SMD placements only or in mixed applications to place bare dies along with SMDs in a single-pass process.

Key benefits at a glance:

- Up to 46,000 flip chip components per hour
- Up to 30,000 die attach components per hour
- Up to 126,500 SMD components per hour (benchmark)
- Processes supported: flip chip, die attach, SMD placement
- 0201 metric capability
- Wafer sizes: 4" to 12"
- 12"/8" wafer stretcher
- Hoop ring handling capability
- Linear dipping unit (LDU 2 X)
- Horizontal wafer system with automatic wafer exchange
- Multi-die capability

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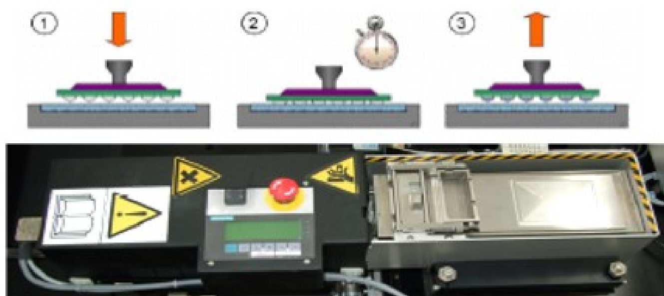
SIPLACE Wafer System SWS

The SIPLACE Wafer System (SWS) enables the SIPLACE CA to combine the direct placement of dies from wafers along with the standard SMT placement process. With its unique single-platform concept, it supports the direct die attach processes as well as the flip chip process.The scalability of the platform optimizes the placement cost for different packages like RF-MCM, FCIP, FC-MLF, FC-CSP.

- Horizontal system
- Max. wafer size: 12"
- 8"/12" wafer stretcher
- Hoop ring handling
- Wafer Map Support
- Auto. wafer exchange
- Multi-die capability
- Min. die thickness: t ≥ 50 µm (silicon)
- Die size: 0.5 to 15 mm

Low force placement

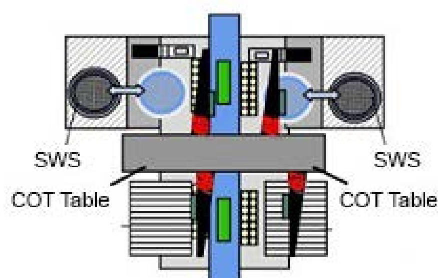
- Touchless pickup, touchless placement and 0.5N placement force features to minimises stress of sensitive components/dies



Linear Dipping Unit (LDU 2 X)

- Accurate and reliable dipping height:
- Flux height accuracy: ± 5 µm
- Flux refill sensor (optional)
- Programmable flux application speed
- Programmable dwell time

The SIPLACE CA enables the exchange between the SWS and a feeder changeover table. New products or change in delivery formats (e.g., wafer, FCO table) can be easily adopted in any combination of COT and SWS as the sum equal to 4.



Sample configuration of SIPLACE CA

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TECHNICAL DATA					
	Flip Chip		**Die Attach**		**SMD**
Accuracy	Wafer Lane Conveyor	Panel Lane Conveyor	Wafer Lane Conveyor	Panel Lane Conveyor	
	±10µm/3σ [a),b)]	±12µm/3σ [a),b)]	±10µm/3σ [a),b)]	±12µm/3σ [a),b)]	±15 µm/3σ [b)]
Throughput in cph (benchmark) [c)]	46,000 with 4 SWS		30,000 with 4 SWS		126,500 with 4 COTs
Die/component sizes	0.5 – 15.0 mm		0.8 – 15.0 mm (smaller on request)		0.11mm -15.0 mm
Die thickness min. (silicon)	50 µm		50 µm		n/a
Bump size min.	25 µm		n/a		n/a
Bump pitch min.	50 µm		n/a		n/a
SIPLACE Wafer System SWS	Horizontal system, automatic wafer exchange, MCM				n/a
SWS wafer size	4" to 12"				n/a
Wafer stretcher	12"/8“ (6" and 4" on request)				n/a
Wafer stretch range	2 mm to 8 mm				n/a
Die eject system	Programmable eject speed				n/a
Linear Dipping Unit LDU 2 X	Free programmable flux application speed				
Flux viscosity	3,000 to 100,000 cps				
Flux height accuracy	± 5 µm				
Programmable bond force	Touchless, 0.5 N to 15.0 N (depending on head)				
Substrate types	FR4, ceramics, flex, boats, 8"/12" wafers, others				
Substrate thickness	0.3 mm to 4.5 mm				
Substrate range	50 x 50 mm to 685 x 650 mm (depending on conveyor types)				
Conveyor types	Flexible dual, Single lane, Wafer lane and Panel lane conveyors				
Transport modes	Synchronous, asynchronous				
Dimension with SWS (WxDxH)	3778mm x 2100mm x 1835				
Supply voltage	3 x 400 VAC~ ± 5%; 50/60 Hz				

Please note that different values stated above may not be possible in all combinations.

a) On-demand for placement process with CP20M2 placement head

b) Based on standard SIPLACE machine capability test

c) Based on SIPLACE SpeedStar

Detailed Specification value available from specification booklet

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